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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/003,933	10/23/2001	Keiichi Yabusaki	6635-60417 (7742.18)	4708

7590 12/17/2004

COUDERT BROTHERS LLP
600 Beach Street, Third Floor
San Francisco, CA 94109

EXAMINER

QUINTO, KEVIN V

ART UNIT	PAPER NUMBER
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2826

DATE MAILED: 12/17/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/003,933

Applicant(s)

YABUSAKI ET AL.

Examiner

Kevin Quinto

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 30 April 2002.
2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-49 is/are pending in the application.
4a) Of the above claim(s) _____ is/are withdrawn from consideration.
5) ☒ Claim(s) 22-49 is/are allowed.
6) ☒ Claim(s) 1-4 and 9-13 is/are rejected.
7) ☒ Claim(s) 5-8 and 14-21 is/are objected to.
8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☒ The specification is objected to by the Examiner.
10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Information Disclosure Statement

1. If the applicant is aware of any relevant prior art, he/she is requested to cite it on form PTO-1449 in accordance with the guidelines set forth in M.P.E.P. 609.

Specification

2. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000.

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Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

4. Claims 1-4, 9, 10, 12, and 13 are rejected under 35 U.S.C. 102(b) as being anticipated by Morishima (USPN 5,291,033).

5. In reference to claims 1-4, Morishima (USPN 5,291,033) discloses a similar device. Figure 13 of Morishima illustrates a semiconductor device with a multiple layered ridge. A first semiconductor layer (100) forms a bottom part of the ridge. A second semiconductor layer (102) is disposed above the first semiconductor layer (100). A third semiconductor layer (104) is disposed above the second semiconductor layer (102). The examiner notes the claim limitations concerning the etching speeds of the three semiconductor layers. However this places claims 1-4 into the form of **product-by-process claims**:

Note that a "product by process" claim is directed to the product per se, no matter how actually made, *In re Hirao*, 190 USPQ 15 at 17 (footnote 3). See also *In re Thorpe*, 227 USPQ 964, 966; *In re Luck*, 177 USPQ 523; *In re Fessmann*, 180 USPQ 324; *In re Avery*, 186 USPQ 161; *In re Wertheim*, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); and *In re Marosi et al.*, 218 USPQ 289, all of which make it clear that it is the patentability of the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or not. Note that applicant has the burden of proof in such cases, as the above case law makes clear. See also MPEP 2113.

Claims 1-4 do not distinguish over the Morishima reference regardless of the process used to etch the three semiconductor layers, because only the final product is relevant, and not the process of making such using a first etchant which has different etching speeds for each of the three semiconductor layers.

6. With regard to claims 9 and 10, the second semiconductor layer (102) meets this claim since it has a thickness of 0.1 μm or 100 nm (column 5, lines 41-43).

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7. In reference to claim 12, both the first semiconductor layer (100) the third semiconductor layer (104) have a thickness of 2 μm or 2000 nm (column 5, lines 36-40 and 45-47) thereby meeting the limitation of the claim.

8. With regard to claim 13, Morishima discloses a similar process. Figures 13-17 illustrate the process of forming a semiconductor device having a multiple layered ridge. A first semiconductor layer (100) forms a bottom part of the ridge. A second semiconductor layer (102) is disposed above the first semiconductor layer (100). A third semiconductor layer (104) is disposed above the second semiconductor layer (102). Morishima discloses (column 6, lines 6-10) the use of a first etchant which etches through the first semiconductor layer (100) at a first etching speed, the second semiconductor layer (102) at a second etching speed, and the third semiconductor layer (104) at a third etching speed wherein the second etching speed is higher than the first etching speed and slower than the third etching speed.

9. Claims 1-4 and 9 are rejected under 35 U.S.C. 102(e) as being anticipated by Nishikata et al. (USPN 6,177,710 B1).

10. In reference to claims 1-4, Nishikata et al. (USPN 6,177,710 B1, hereinafter referred to as the "Nishikata" reference) discloses a similar device. Figures 9 and 10 of Nishikata each illustrate a semiconductor device with a multiple layered ridge. A first semiconductor layer (34) forms a bottom part of the ridge. A second semiconductor layer (35) is disposed above the first semiconductor layer (34). A third semiconductor layer (36) is disposed above the second semiconductor layer (35). The examiner notes

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the claim limitations concerning the etching speeds of the three semiconductor layers.

However this places claims 1-4 into the form of **product-by-process claims**:

Note that a "product by process" claim is directed to the product per se, no matter how actually made, *In re Hirao*, 190 USPQ 15 at 17 (footnote 3). See also *In re Thorpe*, 227 USPQ 964, 966; *In re Luck*, 177 USPQ 523; *In re Fessmann*, 180 USPQ 324; *In re Avery*, 186 USPQ 161; *In re Wertheim*, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); and *In re Marosi et al.*, 218 USPQ 289, all of which make it clear that it is the patentability of the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or not. Note that applicant has the burden of proof in such cases, as the above case law makes clear. See also MPEP 2113.

Claims 1-4 do not distinguish over the Nishikata reference regardless of the process used to etch the three semiconductor layers, because only the final product is relevant, and not the process of making such using a first etchant which has different etching speeds for each of the three semiconductor layers.

11. With regard to claim 9, the second semiconductor layer (35) meets this claim since it has a thickness of 2.1 μm or 201 nm (column 5, lines 41-43).

Claim Rejections - 35 USC § 103

12. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

13. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Morishima (USPN 5,291,033).

14. With regard to claim 11, Morishima teaches all of the claimed invention except for the exact thickness of the second semiconductor layer. Although the Morishima device

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does not teach the exact thickness of the second semiconductor layer as that claimed by Applicant:

The shape, size, dimension differences are considered obvious design choices and are not patentable unless unobvious or unexpected results are obtained from these changes. It appears that these changes produce no functional differences and therefore would have been obvious. Note *In re Leshin*, 125 USPQ 416.

Therefore claim 11 is not patentably distinguishable over the Morishima reference.

15. Claims 10-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nishikata et al. (USPN 6,177,710 B1).

16. With regard to claims 10-12, Nishikata teaches all of the claimed invention except for the exact thickness of the first, second, and third semiconductor layers. Although the Nishikata device does not teach the exact thickness of the first, second, and third semiconductor layers as that claimed by Applicant:

The shape, size, dimension differences are considered obvious design choices and are not patentable unless unobvious or unexpected results are obtained from these changes. It appears that these changes produce no functional differences and therefore would have been obvious. Note *In re Leshin*, 125 USPQ 416.

Therefore claims 10-12 are not patentably distinguishable over the Nishikata reference.

Allowable Subject Matter

17. Claims 22-49 are allowed.

18. Claims 5-8 and 14-21 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

19. The following is a statement of reasons for the indication of allowable subject matter: the examiner is unaware of any semiconductor device having a three

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semiconductor layer forward mesa structure such that the bottom semiconductor layer has a composition of $\text{Al}_{x_1}\text{Ga}_{1-x_1}\text{As}$ where x_1 is constant, the middle semiconductor layer has a composition of $\text{Al}_{x_2}\text{Ga}_{1-x_2}\text{As}$ where x_2 increases from the bottom surface to the top surface of the middle semiconductor layer but is less than or equal to x_1 , and the top semiconductor layer has a composition of $\text{Al}_{x_3}\text{Ga}_{1-x_3}\text{As}$ where x_3 is substantially less than the lowest value of x_2 .

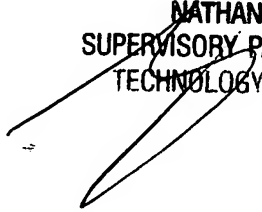
Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kevin Quinto whose telephone number is (571) 272-1920. The examiner can normally be reached on M-F 8AM-5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (571) 272-1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

KVQ


NATHAN J. FLYNN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800